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EXAMINER
CHU, CHRIS C

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 06/04/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Acti n Summary	Application No. 09/677,291	Applicant(s) TABRIZI, BEHNAM	
	Examiner Chris C. Chu	Art Unit 2815	

-- The MAILING DATE of this c mmunication appears on the cover sheet with the c rrespondence address --

Period f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 March 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 39* is/are pending in the application.

4a) Of the above claim(s) *23 - 31 and 37 - 39* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 22 and 32 - 36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 October 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *05 March 2002* is: a)☐ approved b)☒ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Revi w (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Applicant's amendment field on March 5, 2002 has been received and entered in the case.

Drawings

2. The proposed drawing correction filed on March 5, 2002 has been disapproved because it is not in the form of a pen-and-ink sketch showing changes in red ink or with the changes otherwise highlighted. See MPEP § 608.02(v).

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: on page 7, line 6 of the specification refers to a planarizing dielectric material "550" which is not referenced in the figures. Correction is required.

4. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "520" on page 7, line 5 of the amended specification has been used to designate both bare die and device. Correction is required.

5. Applicant is required to submit a proposed drawing correction in reply to this Office action. However, formal correction of the noted defect can be deferred until the application is allowed by the examiner.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

7. Claims 1 ~ 3, 5 ~ 22, and 32 ~ 36 are rejected under 35 U.S.C. 102(e) as being anticipated by Wyland.

Note Fig. 1 of Wyland, where he/she shows an electronic component comprising: a silicon package having a recess (see Fig. 1), the recess including a conductive region (25); and a bare die electronic device (30) having a top, a bottom, sides, and a plurality of terminals, including a non-top terminal, the device being disposed in the recess (see Fig. 1), and wherein the non-top terminal is electrically coupled to the conductive region (see Fig. 1).

Regarding claim 2, Wyland discloses the conductive region (25) is formed by metallization (40 and 25 in Fig. 1).

Regarding claim 3, Wyland discloses the metallization (40 and 25 in Fig. 1), which is achieved through a deposition process. Further, as to the language on line 2 of claim 3, "achieved through a deposition process", even though product-by-process claims are limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process. In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985) (citations omitted). A "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, **190 USPQ 15 at 17** (footnote 3). See also In re Brown, **173 USPQ 685**: In re Luck, **177 USPQ 523**; In re Fessmann, **180 USPQ 324**: In re Avery, **186 USPQ 116**; In re Wertheim, **191 USPQ 90 (209 USPQ 254** does not deal with this issue); and In re Marosi et al., **218 USPQ 289** final product per se which must be determined in a "product by, all of" claim, and not the patentability of the process, and that an old or obvious product, whether claimed in "product by process" claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

Regarding claim 5, Wyland discloses the device (30) is physically coupled to the package by the conductive region (see Fig. 1).

Regarding claim 6, Wyland discloses a dielectric (under 45 in Fig. 1) that is deposited so as to at least partially fill the recess (see Fig. 1 and read column 10, lines 46 ~ 49).

Regarding claim 7, Wyland discloses a plurality of metallized bumps (column 10, lines 39 ~ 40) in a plane, wherein each terminal is electrically coupled to at least one bump, and each bump is electrically coupled to at most one electrically distinct terminal (read column 10, lines 37 ~ 39).

Regarding claim 8, Wyland discloses the package includes a top and a bottom (see Fig. 1); and the bumps (column 10, lines 39 ~ 40) are located above the top of the package (column 10, lines 37 ~ 40).

Regarding claim 9, Wyland discloses the device (30) is a vertical device and the bottom of the device is coupled to the package in the recess (see Fig. 1 and column 10, lines 46 ~ 49).

Regarding claim 10, Wyland discloses a second conductive region (21 in Fig. 1) coupled to a terminal (31 in Fig. 1) other than the non-top terminal (see Fig. 1).

Regarding claim 11, Wyland discloses a plurality of contact (column 10, lines 37 ~ 40) including at least a first contact and a second contact, the first contact being electrically coupled to the non-top terminal and the second contact being electrically coupled to a terminal other than the non-top terminal (see Fig. 1 and read column 10, lines 37 ~ 40).

Regarding claim 12, Wyland discloses the plurality of contacts reside in the same plane (read column 10, lines 37 ~ 40).

Regarding claim 13, Wyland discloses a second layer of dielectric (45 in Fig. 1) completely covering the silicon package and the device except for the plurality of contacts (see Fig. 1).

Regarding claim 14, note Fig. 1 of Wyland, where he/she shows an electronic component comprising: a package having a recess (see Fig. 1), the recess including a first deposition-

processed conductive region (25); and a bare die electronic device (30) having a top, a bottom, sides, and a plurality of terminals, including a non-top terminal and a top terminal, the device being disposed in the recess (see Fig. 1), wherein the non-top terminal is electrically coupled to the conductive region (see Fig. 1) and the top terminal is mechanically coupled to a second deposition-processed conductive region (see Fig. 1) wherein at least a portion of the first and second conductive regions are essentially planar (see Fig. 1). Further, as to the language on lines 2 ~ 3 and lines 7 ~ 8 of claim 14, "deposition-processed conductive region", even though product-by-process claims are limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process. In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985) (citations omitted). A "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, **190 USPQ 15 at 17** (footnote 3). See also In re Brown, **173 USPQ 685**: In re Luck, **177 USPQ 523**; In re Fessmann, **180 USPQ 324**: In re Avery, **186 USPQ 116**; In re Wertheim, **191 USPQ 90 (209 USPQ 254** does not deal with this issue); and In re Marosi et al., **218 USPQ 289** final product per se which must be determined in a "product by, all of" claim, and not the patentability of the process, and that an old or obvious product, whether claimed in "product by process" claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

Regarding claim 15, Wyland discloses the second conductive region (21 in Fig. 1) is a solder bump (read column 10, lines 36 ~ 39).

Regarding claim 16, note Fig. 1 of Wyland, where he/she shows an electronic component comprising: a silicon package having a recess (see Fig. 1), the recess including a conductive region (25 and see Fig. 1); and an electronic device (30) having a top, a bottom, sides, and a plurality of terminals, including a non-top terminal located in a region other than the top of the device, the device being disposed in the recess (see Fig. 1), wherein the non-top terminal is electrically coupled to the conductive region (see Fig. 1).

Regarding claim 17, Wyland discloses one of the terminals (31 in Fig. 1) of the device (30 in Fig. 1) is a top contact located at the top of the device (see Fig. 1); and the package (10) has a package top, wherein the package top also includes a contact coupled electrically via (22) the conductive region to the non-top terminal (see Fig. 1 and read column 10, lines 46 ~ 49).

Regarding claim 18, Wyland discloses the conductive region (25 in Fig. 1) comprises a layer of metal (25 in Fig. 1); and the electronic device (30 in Fig. 1) resides within the recess and the metal is electrically coupled to the bottom terminal of the device (see Fig. 1).

Regarding claim 19, Wyland discloses a layer of insulation (45 in Fig. 1) coupling the silicon package to the electronic device (see Fig. 1 and read column 10, lines 46 ~ 49).

Regarding claim 20, Wyland discloses the metal (25 in Fig. 1) of the conductive region extends to a portion of the package top (see Fig. 1), the electronic component further comprising: a bottom contact electrically coupled to the metal on the package top (see Fig. 1).

Regarding claim 21, note Fig. 1 of Wyland, where he/she shows an electronic component comprising: an electronic device (30) having a first terminal and a second terminal, wherein a first dimension is defined therebetween (see Fig. 1); a silicon package having a first surface and a second surface, the silicon package having a recess on the first surface that has a depth that is

substantially equal to the first dimension (see Fig. 1), the silicon package further having a layer of metal (25) applied to the recess and a portion of the first surface (see Fig. 1), wherein the electronic device resides within the recess (see Fig. 1) and the second terminal is coupled to the metal (see Fig. 1); and a layer of insulation (45) coupling the electronic device to the silicon package (see Fig. 1).

Regarding claim 22, Wyland discloses a first contact (between 31 and 21 in Fig. 1) coupled to the first terminal (31 in Fig. 1); and a second contact (between 30 and 25) coupled to the metal (25 in Fig. 1) residing on the first surface of the silicon package.

Regarding claim 32, note Fig. 1 of Wyland, where he/she shows an electronic component comprising: a non-molded package having a package top and a recess (see Fig. 1); a planar bare die electronic device (30) having a top, a bottom, sides, and a plurality of contacts, the device being disposed in the recess (see Fig. 1); and a planarizing material (45) filling the recess not occupied by the device to substantially create a level plane that includes the top of the device (see Fig. 1). Further, as to the language on line 2 of claim 32, "a non-molded package", even though product-by-process claims are limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process. In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985) (citations omitted). A "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, **190 USPQ 15 at 17** (footnote 3). See also In re Brown, **173 USPQ 685**: In re Luck, **177 USPQ 523**; In re Fessmann, **180 USPQ 324**: In re Avery, **186 USPQ 116**; In re Wertheim, **191**

USPQ 90 (209 USPQ 254 does not deal with this issue); and In re Marosi et al., **218 USPQ 289** final product per se which must be determined in a "product by, all of" claim, and not the patentability of the process, and that an old or obvious product, whether claimed in "product by process" claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

Regarding claim 33, since Wyland does not limit the package to any particular or specific material, his/her disclosure encompasses all well known material's including "silicon."

Regarding claim 34, Wyland discloses a metallization layer (column 10, lines 37 ~ 38 and 25 in Fig. 1).

Regarding claim 35, Wyland discloses the metallization layer (column 10, lines 37 ~ 38 and 25 in Fig. 1) couples each contact to a redistribution point on the package top, and each contact remains electrically distinct (see Fig. 1).

Regarding claim 36, Wyland discloses a plurality of conductive bumps (column 10, lines 39 ~ 40), each bump being disposed at a redistribution point (column 10, lines 37 ~ 40).

8. Claims 1, 14, 16, 21, and 32 are rejected under 35 U.S.C. 102(e) as being anticipated by Suzuki et al.

Note Fig. 1 of Suzuki et al., where he/she shows an electronic component comprising: a silicon package having a recess (1c), the recess including a conductive region (1); and a bare die electronic device (7) having a top, a bottom, sides, and a plurality of terminals, including a non-top terminal, the device being disposed in the recess (see Fig. 1), and wherein the non-top terminal is electrically coupled to the conductive region (see Fig. 1).

Regarding claim 14, note Fig. 1 of Suzuki et al., where he/she shows an electronic component comprising: a package having a recess (1c), the recess including a first deposition-processed conductive region (1); and a bare die electronic device (7) having a top, a bottom, sides, and a plurality of terminals, including a non-top terminal and a top terminal, the device being disposed in the recess (see Fig. 1), wherein the non-top terminal is electrically coupled to the conductive region (see Fig. 1) and the top terminal is mechanically coupled to a second deposition-processed conductive region (see Fig. 1) wherein at least a portion of the first and second conductive regions are essentially planar (see Fig. 1). Further, as to the language on lines 2 ~ 3 and lines 7 ~ 8 of claim 14, "deposition-processed conductive region", even though product-by-process claims are limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process. In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985) (citations omitted). A"product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, **190 USPQ 15 at 17** (footnote 3). See also In re Brown, **173 USPQ 685**: In re Luck, **177 USPQ 523**; In re Fessmann, **180 USPQ 324**: In re Avery, **186 USPQ 116**; In re Wertheim, **191 USPQ 90 (209 USPQ 254** does not deal with this issue); and In re Marosi et al., **218 USPQ 289** final product per se which must be determined in a "product by, all of" claim, and not the patentability of the process, and that an old or obvious product, whether claimed in "product by process" claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

Regarding claim 16, note Fig. 1 of Suzuki et al., where he/she shows an electronic component comprising: a silicon package having a recess (1c), the recess including a conductive region (1); and an electronic device (7) having a top, a bottom, sides, and a plurality of terminals, including a non-top terminal located in a region other than the top of the device, the device being disposed in the recess (see Fig. 1), wherein the non-top terminal is electrically coupled to the conductive region (see Fig. 1).

Regarding claim 21, note Fig. 1 of Suzuki et al., where he/she shows an electronic component comprising: an electronic device (7) having a first terminal and a second terminal, wherein a first dimension is defined therebetween (see Fig. 1); a silicon package having a first surface and a second surface, the silicon package having a recess (1c) on the first surface that has a depth that is substantially equal to the first dimension (see Fig. 1), the silicon package further having a layer of metal (1) applied to the recess and a portion of the first surface (see Fig. 1), wherein the electronic device resides within the recess (see Fig. 1) and the second terminal is coupled to the metal (see Fig. 1); and a layer of insulation (10) coupling the electronic device to the silicon package (see Fig. 1).

Regarding claim 32, note Fig. 1 of Suzuki et al., where he/she shows an electronic component comprising: a non-molded package having a package top and a recess (see Fig. 1); a planar bare die electronic device (7) having a top, a bottom, sides, and a plurality of contacts, the device being disposed in the recess (see Fig. 1); and a planarizing material (10) filling the recess not occupied by the device to substantially create a level plane that includes the top of the device (see Fig. 1). Further, as to the language on line 2 of claim 32, "a non-molded package", even though product-by-process claims are limited by and defined by the process, determination of

patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process. In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985) (citations omitted). A "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, **190 USPQ 15 at 17** (footnote 3). See also In re Brown, **173 USPQ 685**: In re Luck, **177 USPQ 523**; In re Fessmann, **180 USPQ 324**: In re Avery, **186 USPQ 116**; In re Wertheim, **191 USPQ 90 (209 USPQ 254** does not deal with this issue); and In re Marosi et al., **218 USPQ 289** final product per se which must be determined in a "product by, all of" claim, and not the patentability of the process, and that an old or obvious product, whether claimed in "product by process" claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

9. Claims 1, 14, 16, 21, and 32 are rejected under 35 U.S.C. 102(b) as being anticipated by Andros et al. or Corisis or Hernandez et al. or Hebert.

Andros et al. or Corisis or Hernandez et al. or Hebert discloses an electronic component comprising: a silicon package having a recess, the recess including a conductive region; and a bare die electronic device having a top, a bottom, sides, and a plurality of terminals, including a non-top terminal, the device being disposed in the recess, and wherein the non-top terminal is electrically coupled to the conductive region.

Regarding claim 14, Andros et al. or Corisis or Hernandez et al. or Hebert discloses an electronic component comprising: a package having a recess, the recess including a first

deposition-processed conductive region; and a bare die electronic device having a top, a bottom, sides, and a plurality of terminals, including a non-top terminal and a top terminal, the device being disposed in the recess, wherein the non-top terminal is electrically coupled to the conductive region and the top terminal is mechanically coupled to a second deposition-processed conductive region wherein at least a portion of the first and second conductive regions are essentially planar. Further, as to the language on lines 2 ~ 3 and lines 7 ~ 8 of claim 14, "deposition-processed conductive region", even though product-by-process claims are limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process. In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985) (citations omitted). A"product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, **190 USPQ 15 at 17** (footnote 3). See also In re Brown, **173 USPQ 685**: In re Luck, **177 USPQ 523**; In re Fessmann, **180 USPQ 324**: In re Avery, **186 USPQ 116**; In re Wertheim, **191 USPQ 90 (209 USPQ 254** does not deal with this issue); and In re Marosi et al., **218 USPQ 289** final product per se which must be determined in a "product by, all of" claim, and not the patentability of the process, and that an old or obvious product, whether claimed in "product by process" claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

Regarding claim 16, Andros et al. or Corisis or Hernandez et al. or Hebert discloses an electronic component comprising: a silicon package having a recess, the recess including a conductive region; and an electronic device having a top, a bottom, sides, and a plurality of

terminals, including a non-top terminal located in a region other than the top of the device, the device being disposed in the recess, wherein the non-top terminal is electrically coupled to the conductive region.

Regarding claim 21, Andros et al. or Corisis or Hernandez et al. or Hebert discloses an electronic component comprising: an electronic device having a first terminal and a second terminal, wherein a first dimension is defined therebetween; a silicon package having a first surface and a second surface, the silicon package having a recess on the first surface that has a depth that is substantially equal to the first dimension, the silicon package further having a layer of metal applied to the recess and a portion of the first surface, wherein the electronic device resides within the recess and the second terminal is coupled to the metal; and a layer of insulation coupling the electronic device to the silicon package.

Regarding claim 32, Andros et al. or Corisis or Hernandez et al. or Hebert discloses an electronic component comprising: a non-molded package having a package top and a recess; a planar bare die electronic device having a top, a bottom, sides, and a plurality of contacts, the device being disposed in the recess; and a planarizing material filling the recess not occupied by the device to substantially create a level plane that includes the top of the device. Further, as to the language on line 2 of claim 32, "a non-molded package", even though product-by-process claims are limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process. In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985) (citations omitted). A "product by process" claim is

directed to the product per se, no matter how actually made, In re Hirao, **190 USPQ 15 at 17** (footnote 3). See also In re Brown, **173 USPQ 685**: In re Luck, **177 USPQ 523**; In re Fessmann, **180 USPQ 324**: In re Avery, **186 USPQ 116**; In re Wertheim, **191 USPQ 90 (209 USPQ 254** does not deal with this issue); and In re Marosi et al., **218 USPQ 289** final product per se which must be determined in a "product by, all of" claim, and not the patentability of the process, and that an old or obvious product, whether claimed in "product by process" claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wyland or Suzuki et al. or Andros et al. or Corisis or Hernandez et al. or Hebert in View of Yoshida et al. or Oji et al.

Wyland or Suzuki et al. or Andros et al. or Corisis or Hernandez et al. or Hebert discloses all of the claimed invention except the conductive region comprises: a first layer of titanium; a second layer of copper deposited on the first layer; and a third layer of chrome deposited on the second layer. However, Yoshida et al. or Oji et al. discloses the conductive region comprises: a first layer of titanium; a second layer of copper deposited on the first layer; and a third layer of

chrome deposited on the second layer. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Wyland or Suzuki et al. or Andros et al. or Corisis or Hernandez et al. or Hebert by adding the conductive region as taught by Yoshida et al. or Oji et al. The ordinary artisan would have been motivated to modify Wyland or Suzuki et al. or Andros et al. or Corisis or Hernandez et al. or Hebert in the manner described above for at least the purpose of increasing adhesive strength between the conductive region and the device.

Response to Arguments

12. Applicant's arguments filed March 5, 2002 have been fully considered but they are not persuasive.

For Wyland:

On page 6, applicant argues "a non-top terminal is neither taught nor suggested in Wyland." The argument is not persuasive. First, "terminal" is defined in Merriam-Webster's Collegiate Dictionary, 10th ed., page 1212 a device attached to the end of a wire or cable or to an electrical apparatus for convenience in making connections. Second, a die is an electrical apparatus and formed by a multi layers. Thus, the bottom layer of die is a device which is attached to the end of an electrical apparatus for the convenience in making connections. Therefore, Wyland discloses a non-top terminal (the bottom layer of die).

Further, applicant argues "a non-top terminal is electrically coupled to the conductive region, as required in claim 1, is neither taught nor suggested in the Wyland." Examiner does not

concur. Wyland uses a silver-filled epoxy adhesive to attach the die 30 to the die attach paddle 25 (column 5, lines 41 ~ 44). The silver-filled epoxy adhesive is an electrically conductive material (read Hernandez, U.S. Pat. No. 4989117, in column 7, lines 37 ~ 39) to establish an electrical and thermal connection between the lower surface of the die and the upper contact area of die attach paddle. Since the die attach paddle is connected to the output terminals such as leads or lead fingers 21, the die attach paddle contains electricity. Therefore, Wyland discloses the limitation, the non-top terminal (the bottom layer of die) being electrically coupled to the conductive region (25), as required in claim 1.

Furthermore, applicant argues "Wyland does not disclose a silicon package having a recess in which a bare die electronic device is disposed, as required by claim 1." The argument is not persuasive. Wyland discloses a semiconductor package which is an equivalent structure in the art as known as silicon package. Therefore, Wyland discloses a silicon package (the structure in Fig. 1) having a recess (the place of 25) in which a bare die (30) electronic device is disposed, as required by claim 1.

Even further, applicant argues "[A] package having a recess on the first surface that has a depth that is substantially equal to the first dimension, as required by claim 21, is neither taught nor suggested by Wyland." The argument is not persuasive. Since the term "substantially equal" used to define the depth of the recess allows flexibility in the actual length of the depth, Wyland discloses in Fig. 1 that the depth of recess is substantially equal to the first dimension.

Finally, applicant argues "planarizing material filling the recess not occupied by the device to substantially create a level plane that includes the top of the device is neither taught nor suggested by Wyland." Examiner does not concur. Since the term "level plane" is not defined

specifically in the claims, any plane is read as "level plane." Therefore, Wyland discloses in Fig. 1 planarizing material (45) filling the recess not occupied by the device to substantially create a level plane that includes the top of the device.

At last, the rejections by the Suzuki et al., Andros et al., Corisis, Hernandez et al. and Hebert are maintained for the same reasons as explained under Wyland.

Conclusion

13. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is (703) 305-6194. The examiner can normally be reached on M-F (10:30 - 7:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (703) 308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7382 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Chris C. Chu
Examiner
Art Unit 2815

c.c.
May 30, 2002

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800